Automatic Layout Synthesis For High-performance Full Custom VLSI Chips (Report) By Jaewon Kim

By Jaewon Kim

Volume 6521 Improving the power-performance of multicore processors through optimization of lithography and thermal processing Ju-Byung Kim
http://spie.org/Publications/Proceedings/Volume/6521

EDA for IC Implementation, Circuit Design, and Process Technology Electronic Design Automation for Integrated Circuits Handbook Edited by Louis Scheffer, Luciano
https://www.scribd.com/doc/268827032/Electronic-design-automation-for-integrated-circuits-handbook-Luciano-Lavagno-Louis-Scheffer-Grant-Martin-EDA-for-IC-implementation-circuit-desig

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http://www.dtic.mil/dtic/tr/fulltext/u2/a121365.pdf

PTL has been recognized as one of the potential alternatives to static CMOS for the synthesis of high performance layout, the design of chips Full-custom
http://dl.acm.org/citation.cfm?doid=1119772.1119813

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It attains high performance by the system generates automatically the corresponding layout in a full custom Array optimization for VLSI synthesis:
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http://fr.slideshare.net/jainatush/cmos-digital-integrated-circuits-analysis-and-design

IEEE Xplore. Delivering full text Synthesis for high performance The performance improvement process involves interaction between the layout tool and some of
http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=112230&isnumber=3356

Automatic Layout Generation of High Performance rated all steps to generate a high-performance layout of a D/A converter. automatic layout generation
http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.23.4848&rep=rep1&type=pdf

This paper presents a methodology towards synthesis of high performance analog circuits. Layout parasitics are estimated and compensated during circuit sizing.
http://citeseerx.ist.psu.edu/showciting?cid=2166872

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http://www.amazon.com/Automatic-layout-synthesis-high-performance-custom/dp/B0006QBLG0

Automatic Layout Generation physical level layouts that have high performance and the automatic mapping of CMOS functions into a
http://www.academia.edu/10423716/Automatic_Layout_Generation

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GEMS: an automatic layout tool for structural description into full custom VLSI layout. the incremental symbolic synthesis of high performance VLSI
http://dl.acm.org/citation.cfm?doid=318013.318034

Proceedings of SPIE Volume 7275 on sale Qi-Zhong Hong; T. S. Kim; Ricardo Borges; full-chip analysis
http://spie.org/Publications/Proceedings/Volume/7275

The Computer Engineering Handbook is Although automatic synthesis of logic circuits are widely used in today s very large scale integration (VLSI) chips.
http://www.calameo.com/books/00016841120aa4b9944d3

Folding Transistor sizing is essential to produce high performance fully automatic layout synthesis system for standard Layout Synthesis with
http://www.academia.edu/7073809/Automatic_Layout_Synthesis_with_ASTRAN_Applied_to_Asynchronous_Cells

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A systematic method for automatic layout synthesis of circuit performance optimization. These layout using circuit recognition and constraint
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http://link.springer.com/chapter/10.1007%2F0-306-47823-4_4

IC Layout Basics : A Practical Guide Saint, High Performance Devices : Unleash the Full Potential of Google Sherman, Chris
http://info.ifpan.edu.pl/ACTIVITY/i_Engineering_200810.xls

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